REMARKS

Preliminary Matter

Applicants thank the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119 and receipt of the certified copy of the priority document. Applicants also thank the Examiner for considering the references cited with the Information Disclosure Statements (IDS) filed on January 13, 2006 and February 23, 2006.

Applicants note that the Examiner did not indicate whether the drawings have been accepted. Accordingly, Applicants respectfully request that the Examiner check the proper box on the PTOL-326 (Office Action Summary) of the next office paper to indicate that the drawings have been accepted.

Status of the Application

Claims 1-6, 8 and 11-15 have been examined and are all the claims pending in the application. Claims 5, 6, 12, and 15 are amended for reasons of precision of language. It is respectfully submitted that these amendments were made merely to more accurately claim the present invention and do not implicate estoppel in the application of the doctrine of equivalents.

Double Patenting

On pages 2-3, the Examiner has seemingly rejected claims 5 under 35 U.S.C. § 101 for double patenting, alleging that claim 5 claims the same invention as that of claim 6. Applicants submit that a double patenting rejection is not appropriate as both claims are in the same application. Thus, withdrawal of the rejection is respectfully requested.

The Examiner has objected to claim 6 under 37 C.F.R. § 1.75 as allegedly being a substantial duplicate of claim 5. Applicants respectfully disagree and traverse this objection.

Claim 5 recites a semiconductor device comprising *a memory block* having a plurality of segments. In contrast, claim 6 recites a semiconductor device comprising *a plurality of memory blocks*, each of which has a plurality of segments. The claims differ in scope, as claim 5 requires only a single memory block, whereas claim 6 requires a plurality of memory blocks. Thus, Applicants submit that claims 5 and 6 are not substantial duplicates of one another and respectfully request withdrawal of the objection.

Claim Rejections - 35 U.S.C. § 102(b) to Nagai

The Examiner has rejected claims 1-6, 8, and 11-15 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent Application Publication No. 2001/0055233 to Nagai (hereinafter "Nagai"). Applicants submit that the claims are patentable.

For example, claim 1 recites that segments having defects are dispersively allocated to a plurality of redundancy memory blocks and replaced by redundancy segments of the allocated redundancy blocks. Each of said plurality of redundancy memory blocks has a redundancy segment which replaces any of the segments having defects.

Nagai is directed to a memory cell array divided in a matrix shape with eight rows and eight columns. Each divided unit is called a segment, the eight segments in each row are called bank 0 to bank 7, and the eight segments in each column form segment arrays seg 0 to seg 7 (paragraph 76). Each segment array has 64 normal column selection lines and two spare column selection lines to be used if a segment contains faulty elements (paragraph 84).

The Examiner seems to contend that the set of normal column selection lines in each segment array correspond to the claimed plurality of memory blocks and that the set of spare selection lines in each segment array corresponds to the claimed plurality of redundancy memory blocks. However, Nagai discloses that if a normal element is faulty, a spare element *in a segment having the faulty element* is used in place of the faulty element (paragraph 87). Thus, Nagai does not teach that *each* of the alleged plurality of redundancy memory blocks (spare selection lines) has an alleged redundancy segment (spare element) which replaces *any* segments having defects (faulty element). Conversely, Nagai's spare elements can *only* repair faulty elements *within the same segment.*

Because Nagai does not teach or suggest all of the features of claim 1, Applicants submit that the claim is patentable and respectfully request withdrawal of the rejection. Applicants also submit that claims 2-4, being dependent on claim 1, are patentable at least by virtue of their dependency.

Independent claims 5 and 6 recite features analogous to those discussed above in conjunction with claim 1. Thus, Applicants submit that these claims are patentable at least for reasons analogous with those discussed above regarding claim 1. Applicants also submit that claims 8 and 11-15, being dependent on one of claims 5 and 6, are patentable at least by virtue of their dependency.

Claim Rejections - 35 U.S.C. § 102(b) to Chung

The Examiner has rejected claims 1-6, 8, and 11-15 under 35 U.S.C. § 102(b) as allegedly being anticipated by U.S. Patent No. 6,154,389 to Chung et al. (hereinafter "Chung"). Applicants submit that the claims are patentable.

For example, claim 1 recites a semiconductor memory device which includes a plurality of memory blocks and a plurality of redundancy memory blocks provided for each of the plurality of memory blocks. Segments having defects among a plurality of segments included in the plurality of memory blocks are dispersively allocated to the plurality of redundancy memory blocks and replaced by the allocated redundancy memory blocks. Also, each of said plurality of redundancy memory blocks has a redundancy segment which replaces any of the segments having defects.

Chung is directed to a flash memory device which has a plurality of mats 100a, 100b, 100c, and 100d corresponding to respective redundancy selection circuits 200a, 200b, 200c, and 200d. Each mat comprises four sectors, each sector having a main memory cell array 110 of main memory cells and a redundancy memory cell array 140 of redundant memory cells for replacing at least one column having faulty cells in the main memory cell array (col. 3, lines 33-43). The main memory cell array 110 includes a plurality of input/output blocks 111, and the redundancy memory cell array 140 includes a plurality of redundant columns each having two redundancy blocks 141_0 and 141_1 (col. 4, lines 8-16 and 37-44). Columns within a bit segment 112_0 or 112_1 of each I/O block 111, and redundancy columns within redundant bit bit segments 142_0 and 142_1 of each redundancy block 141_0 and 141_1 are supplied to

corresponding multiplexers 180, respectively (col. 5, lines 10-19). Each multiplexer 180 outputs either the column within the corresponding bit segment 112_0, 112_1 or the column within the corresponding redundant bit segment 142_0, 142_1 in response to redundancy selection signals from the redundancy selection circuits 200a, 200b, 200c, and 200d (col. 9, lines 22-33).

On page 6 of the Office Action, the Examiner seems to contend that Chung's plurality of mats 100a, 100b, 100c, and 100d correspond to the claimed plurality of memory blocks and that Chung's redundancy selection circuits 200a, 200b, 200c, and 200d correspond to the claimed plurality of redundancy memory blocks. The Examiner further contends that the I/O blocks 111 correspond to the claimed segments. However, Chung's redundancy selection circuits 200a, 200b, 200c, and 200d merely include first and second redundancy flag generators 210, 220 and first and second redundancy selection signal generators 230, 240 (Figure 1B). Chung discloses that these components act only as redundancy block selectors (col. 5, lines 41-47) which select whether data of a column of redundancy blocks 141_0 and 141_1 on DL16 or DL17 is to be output (col. 5, lines 15-26). Thus, Chung does not teach that the alleged segments 111 having defects are dispersively allocated to the alleged plurality of redundancy memory blocks 200a, 200b, 200c, and 200d as required by claim 1. Further, Chung does not teach that the segments 11 having defects are replaced by the alleged plurality of redundancy memory blocks 200a, 200b, 200c, and 200d as required by claim 1.

The Examiner may have more appropriately asserted that Chung's redundancy memory cell arrays 140 in respective sectors correspond to the claimed plurality of redundancy memory blocks, and that Chung's main memory cell arrays 110 in respective sectors correspond to the

claimed plurality of memory blocks. Applicants submit that even if the Examiner were to make this assertion, the limitations of claim 1 would not be met. In col. 7, line 55 to col. 9, line 33, Chung discloses an operation in which a column MBL2 in I/O block 111 of the main memory array 110 is defective and is repaired using redundant column RC3 of redundancy memory cell array 140. Based on a redundancy selection signal nRS0_0, multiplexer 180 will output DL16 holding redundant column RC3 in place of DL0 which holds the defective column MBL2. Chung discloses that if two I/O blocks 111 have defective main columns, the columns are repaired in the same manner (col. 10, lines33-40). Therefore, defective columns are allocated to redundant columns *within the same redundancy memory cell array* 140. Thus, Chung does not teach that segments 111 in a memory block 110 having defects are *dispersively* allocated to a *plurality* of redundancy memory blocks (140 of each sector) as required by claim 1.

Similarly, Chung does not teach that each of the alleged plurality of redundancy memory blocks (140 of each sector) has a redundancy segment (redundant column) which replaces *any* of the segments 111 having defects. In contrast, Chung's redundant columns within each redundant memory cell array 140 of each sector can *only* repair a defective column within that *same* sector.

Because Chung does not teach all of the features of claim 1, Applicants submit that the claim is not anticipated, and respectfully request withdrawal of the rejection. Applicants also submit that claims 2-4, being dependent on claim 1, are patentable at least by virtue of their dependency.

Claim 5 recites a plurality of redundancy memory blocks, each having a redundancy segment which substitutes for any segment having a defect among a plurality of segments in a

memory block. The Examiner seems to contend that Chung's plurality of mats 100a corresponds to the claimed memory block and that Chung's redundancy selection circuits 200a, 200b, 200c, and 200d correspond to the claimed plurality of redundancy memory blocks. As previously mentioned, Chung's redundancy selection circuits 200a, 200b, 200c, and 200d merely include first and second redundancy flag generators 210, 220 and first and second redundancy selection signal generators 230, 240 (Figure 1B). Chung discloses that these components act only as redundancy block selectors (col. 5, lines 41-47). Thus, Chung does not teach that the alleged redundancy segment 210, 220, 230, or 240 substitutes for any segment 111 having a defect among a plurality of segments in a memory block 100.

Furthermore, even if the Examiner had more appropriately asserted that Chung's redundancy memory cell arrays 140 correspond to the claimed plurality of redundancy memory blocks, and that Chung's main memory cell array 110 corresponds to the claimed plurality of memory blocks, the limitations of claim 5 would not be met. As noted above, Chung's redundant columns repair defective columns *within the same redundancy memory cell array* 140. Thus, Chung does not teach that *each* of the alleged plurality of redundancy memory blocks (140 of all sectors) has a redundancy segment (redundant column) which substitutes for *any* segment (defective column in 111) having a defect among the plurality of segments in the memory block 110. Conversely, the redundant columns with each redundant memory cell array 140 of each sector can only repair a defective column within that *same* sector.

Because Chung does not teach or suggest all of the features recited in claim 5, Applicants submit that the claim is patentable and respectfully request withdrawal of the rejection.

Applicants also submit that claims 8, 11, and 12, being dependent on claim 5, are patentable at least by virtue of their dependency.

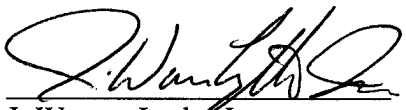
Claim 6 recites features that are analogous to those recited in claim 5 as discussed above. Thus, Applicants submit that claim 6 is patentable at least for reasons analogous to those discussed above in conjunction with claim 5. Applicants also submit that claims 13-15, being dependent on claim 6, are patentable at least by virtue of their dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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